36. The method according to claim 35, wherein the controlled oscillator circuit comprises an inductor-capacitor tank circuit.

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37. The method according to claim 36, wherein the inductor-capacitor tank circuit comprises a capacitor electrically coupled to the first and second inductance circuits.

38. The method according to claim 37, wherein the first and second inductance circuits are formed entirely within the semiconductor package.

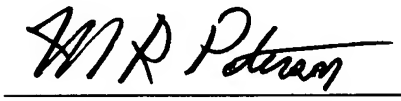
39. The method according to claim 26, wherein the first and second inductance circuits are formed symmetrically with respect to each other.

CONCLUSION

A check in the amount of $324.00 is enclosed for excess claims. Should any additional fees under 37 CFR 1.16-1.21 be required for any reason relating to the enclosed materials, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/SILA:106.

The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,



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APPENDIX

MARKED UP VERSION OF AMENDMENTS AS REQUIRED BY RULE 121

In The Specification:

Please replace the paragraph beginning on page 1, line 24 and ending on page 2, line 2 with the following:

--This patent application claims priority to, and incorporates by reference, the following patent documents: U.S. Patent Application Serial No. [_____] 10/075,094, Attorney Docket No. SILA:074, titled "Radio-Frequency Communication Apparatus and Associated Methods"; U.S. Patent Application Serial No. [_____] 10/075,098, Attorney Docket No. SILA:075, titled "Apparatus and Methods for Generating Radio Frequencies in Communication Circuitry"; and U.S. Patent Application Serial No. [_____] 10/074,591, Attorney Docket No. SILA:096, titled "Apparatus for Generating Multiple Radio Frequencies in Communication Circuitry and Associated Methods."--

On page 2, replace the paragraph at lines 4-16 with:

--Furthermore, this patent application incorporates by reference the following patent documents: U.S. Patent Application Serial No. [_____] 10/075,122, Attorney Docket No. SILA:078, titled "Digital Architecture for Radio-Frequency Apparatus and Associated Methods"; U.S. Patent Application Serial No. [_____] 10/075,099, Attorney Docket No. SILA:097, titled "Notch Filter for

DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods"; U.S. Patent Application Serial No. [_____] 10/074,676, Attorney Docket No. SILA:098, titled "DC Offset Reduction in Radio-Frequency Apparatus and Associated Methods"; U.S. Patent Application Serial No. [_____] 10/079,058, Attorney Docket No. SILA:099, titled "Apparatus and Methods for Output Buffer Circuitry with Constant Output Power in Radio-Frequency Circuitry"; U S. Patent Application Serial No. [_____] 10/081,121, Attorney Docket No. SILA:095, titled "Calibrated Low-Noise Current and Voltage References and Associated Methods"; and U.S. Patent Application Serial No. [_____] 10/079,057, Attorney Docket No. SILA:107, titled "Apparatus and Method for Front-End Circuitry in Radio-Frequency Apparatus."--

On page 25, replace the paragraph at lines 10-22 with:

--The transmit path circuitry shown in FIG. 1D constitutes one possible architecture for a transmit path circuitry that may advantageously use the inventive concepts. As persons of ordinary skill in the art who have the benefit of the description of the invention understand, one may use other transmit path circuitry architectures and circuit arrangements, as desired, for example, direct up-conversion transmit path circuitries, and the like. U.S. Patent Application Serial No. [_____] 10/075,094, Attorney Docket No. SILA:074, titled "Radio-Frequency Communication Apparatus and Associated Methods"; U.S. Patent Application Serial No. [_____] 10/075,098, Attorney Docket No. SILA:075, titled "Apparatus and

Methods for Generating Radio Frequencies in Communication Circuitry"; and U.S. Patent Application Serial No. [_____] 10/074,591, Attorney Docket No. SILA:096, titled "Apparatus for Generating Multiple Radio Frequencies in Communication Circuitry and Associated Methods," incorporated by reference here, describe further details of the transmit path circuitry and its various components in exemplary RF circuitry that can use the invention.--

In The Claims:

1. (Amended) A semiconductor package comprising:

a package substrate having a first surface;

an integrated circuit electrically coupled to the first surface of the package substrate, the integrated circuit and the package substrate together forming the semiconductor package; [and]

a first inductance circuit formed within the semiconductor package; and

a second inductance circuit formed within the semiconductor package,

wherein the first inductance circuit is electrically coupled in parallel to the second inductance circuit, and

wherein the first and second inductance circuits have substantially symmetrical geometric characteristics.

[2.(Canceled) A semiconductor package comprising:

a package substrate having a first surface;

an integrated circuit electrically connected to said first surface of said package substrate, said integrated circuit and said package substrate together forming said semiconductor package, the integrated circuit and package substrate including frequency synthesizer circuitry; and

at least one inductance circuit formed entirely within said semiconductor package and formed at least partially between said integrated circuit and said package substrate, the inductance circuit at least in part determining an output frequency for the frequency synthesizer circuitry;

wherein said frequency synthesizer circuitry has an output frequency selectably operable within a plurality of bands, and wherein said at least one inductance circuit forms part of a controlled oscillator circuit within said frequency synthesizer circuitry, the output frequency being dependent upon the controlled oscillator circuit.]

--3. (New) The semiconductor package according to claim 1, further comprising a phase locked loop circuit included within the integrated circuit.--

--4. (New) The semiconductor package according to claim 3, wherein the phase locked loop circuit comprises a controlled oscillator circuit.--

--5. (New) The semiconductor package according to claim 4, wherein the controlled oscillator circuit has an output frequency that is selectably operable within a plurality of frequency bands.--

--6. (New) The semiconductor package according to claim 5, wherein the controlled oscillator circuit comprises an inductor-capacitor tank circuit.--

--7. (New) The semiconductor package according to claim 6, wherein the inductor-capacitor tank circuit comprises a capacitor electrically coupled to the first and second inductance circuits.--

--8. (New) The semiconductor package according to claim 7, wherein the first and second inductance circuits are formed entirely within the semiconductor package.--

--9. (New) The semiconductor package according to claim 3, wherein the integrated circuit comprises a differential amplifier coupled to the parallel combination of the first and second inductance circuits.--

--10. (New) A semiconductor package, comprising:

a package substrate having a first surface;

an integrated circuit electrically coupled to the first surface of the package substrate;

a first inductance circuit formed within the semiconductor package and formed at least partially between the integrated circuit and the package substrate; and

a second inductance circuit coupled electrically in parallel with the first inductance circuit, the second inductance circuit formed within the semiconductor package and formed at least partially between the integrated circuit and the package substrate,

wherein the first inductance circuit is formed symmetrically with respect to the second inductance circuit.--

--11. (New) The semiconductor package according to claim 10, wherein the first inductance circuit comprises a first substrate electrical contact on the first surface of the package substrate, wherein the first inductance circuit is formed by first and second conductive features electrically coupled between the integrated circuit and the first substrate electrical contact to form an electrically conductive path.--

--12. (New) The semiconductor package according to claim 11, wherein the second inductance circuit comprises a second substrate electrical contact on the first surface of the package substrate, wherein the second inductance circuit is formed by third and fourth conductive features electrically coupled between the integrated circuit and the second substrate electrical contact to form an electrically conductive path.--

--13. (New) The semiconductor package according to claim 12, wherein the package substrate comprises a first set of at least two alternative substrate electrical contacts corresponding to the first inductance circuit to provide alternate electrical connection points during package assembly for at least one or both of the first and second conductive features of the first inductance circuit, an inductance value of the first inductance circuit being dependent on the identity of the alternative substrate electrical contact selected in

the first set of at least two alternative substrate electrical contacts for coupling electrically to at least one or both of the first and second conductive features.--

--14. (New) The semiconductor package according to claim 13, wherein the package substrate comprises a second set of at least two alternative substrate electrical contacts corresponding to the second inductance circuit to provide alternate electrical connection points during package assembly for at least one or both of the third and fourth conductive features of the second inductance circuit, an inductance value of the second inductance circuit being dependent on the identity of the alternative substrate electrical contact selected in the second set of at least two alternative substrate electrical contacts for coupling electrically to at least one or both of the third and fourth conductive features.--

--15. (New) The semiconductor package according to claim 14, wherein the first set of alternative substrate electrical contacts comprises alternative substrate bonding pads disposed at variable distances from the integrated circuit, and wherein the first and second conductive features of the first inductance circuit comprise first and second wire bonds electrically coupled to a selected one of the alternative substrate bonding pads to form an electrically conductive path having an inductance value at least partially dependent on at least one of the lengths of the first and second wire bonds, the distance between the first and second wire bonds, or both.--

--16. (New) The semiconductor package according to claim 15, wherein the second set of alternative substrate electrical contacts comprises alternative substrate bonding pads disposed at variable distances from the integrated circuit, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth wire bonds electrically coupled to a selected one of the alternative substrate bonding pads to form an electrically conductive path having an inductance value at least partially dependent on at least one of the lengths of the third and fourth wire bonds, the distance between the third and fourth wire bonds, or both.--

--17. (New) The semiconductor package according to claim 14, wherein the first set of alternative substrate electrical contacts corresponding to the first inductance circuit comprises alternative pairs of first and second substrate bonding pads positioned at variable locations on or within the package substrate, each of the first and second substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a fifth conductive feature, and wherein the first and second conductive features of the first inductance circuit comprise first and second solder bumps positioned so that they are electrically coupled to a selected respective alternative pair of first and second substrate bonding pads to form an electrically conductive path.--

--18. (New) The semiconductor package according to claim 17, wherein the second set of alternative substrate electrical contacts corresponding to the second inductance circuit

comprises alternative pairs of third and fourth substrate bonding pads positioned at variable locations on or within the package substrate, each of the third and fourth substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a sixth conductive feature, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth solder bumps positioned so that they are electrically coupled to a selected respective alternative pair of third and fourth substrate bonding pads to form an electrically conductive path.--

--19. (New) The semiconductor package according to claim 14, wherein the first set of alternative substrate electrical contacts corresponding to the first inductance circuit comprises alternative pairs of first and second substrate bonding pads positioned at variable locations on or within the package substrate, each of the first and second substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a fifth conductive feature, and wherein the first and second conductive features of the first inductance circuit comprise first and second wire bonds electrically coupled to a selected respective alternative pair of first and second substrate bonding pads to form an electrically conductive path.--

--20. (New) The semiconductor package according to claim 19, wherein the second set of alternative substrate electrical contacts corresponding to the second inductance circuit

comprises alternative pairs of third and fourth substrate bonding pads positioned at variable locations on or within the package substrate, each of the third and fourth substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a sixth conductive feature, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth wire bonds electrically coupled to a selected respective alternative pair of third and fourth substrate bonding pads to form an electrically conductive path.--

--21. (New) The semiconductor package according to claim 14, wherein the integrated circuit comprises a differential amplifier coupled to the parallel combination of the first and second inductance circuits.--

--22. (New) A method of assembling a semiconductor package, comprising:

providing a package substrate having a first surface;

including within the semiconductor package an integrated circuit electrically coupled to the package substrate;

forming a first inductance circuit within the semiconductor package, the first inductance being formed at least partially between the integrated circuit and the package substrate; and

forming a second inductance circuit within the semiconductor package, the second inductance being formed at least partially between the integrated circuit

and the package substrate, the second inductance circuit being coupled electrically in parallel with the first inductance circuit,

wherein the first and second inductance circuits are formed within the semiconductor package so that an interfering magnetic signal induces a common-mode signal in the parallel combination of the first and second inductance circuits.--

--23. (New) The method according to claim 22, wherein forming the first inductance circuit further comprises:

providing a first substrate electrical contact on the first surface of the package substrate; and

coupling electrically first and second conductive features between the integrated circuit and the first substrate electrical contact to form an electrically conductive path.--

--24. (New) The method according to claim 23, wherein forming the second inductance circuit further comprises:

providing a second substrate electrical contact on the first surface of the package substrate; and

coupling electrically third and fourth conductive features between the integrated circuit and the first substrate electrical contact to form an electrically conductive path.--

--25. (New) The method according to claim 24, wherein forming the first inductance circuit further comprises:

including within the package substrate a first set of at least two alternative substrate electrical contacts corresponding to the first inductance circuit to provide alternate electrical connection points during package assembly for at least one or both of the first and second conductive features of the first inductance circuit,

wherein an inductance value of the first inductance circuit depends on the identity of the alternative substrate electrical contact selected in the first set of at least two alternative substrate electrical contacts for coupling electrically to at least one or both of the first and second conductive features.--

--26. (New) The method according to claim 25, wherein forming the second inductance circuit further comprises:

including within the package substrate a second set of at least two alternative substrate electrical contacts corresponding to the second inductance circuit to provide alternate electrical connection points during package assembly

for at least one or both of the third and fourth conductive features of the second inductance circuit,

wherein an inductance value of the second inductance circuit depends on the identity of the alternative substrate electrical contact selected in the second set of at least two alternative substrate electrical contacts for coupling electrically to at least one or both of the third and fourth conductive features.--

--27. (New) The method according to claim 26, wherein the first set of alternative substrate electrical contacts comprises alternative substrate bonding pads disposed at variable distances from the integrated circuit, and wherein the first and second conductive features of the first inductance circuit comprise first and second wire bonds electrically coupled to a selected one of the alternative substrate bonding pads to form an electrically conductive path having an inductance value at least partially dependent on at least one of the lengths of the first and second wire bonds, the distance between the first and second wire bonds, or both.--

--28. (New) The method according to claim 27, wherein the second set of alternative substrate electrical contacts comprises alternative substrate bonding pads disposed at variable distances from the integrated circuit, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth wire bonds electrically coupled to a selected one of the alternative substrate bonding pads to form an electrically

conductive path having an inductance value at least partially dependent on at least one of the lengths of the third and fourth wire bonds, the distance between the third and fourth wire bonds, or both.--

--29. (New) The method according to claim 26, wherein the first set of alternative substrate electrical contacts corresponding to the first inductance circuit comprises alternative pairs of first and second substrate bonding pads positioned at variable locations on or within the package substrate, each of the first and second substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a fifth conductive feature, and wherein the first and second conductive features of the first inductance circuit comprise first and second solder bumps positioned so that they are electrically coupled to a selected respective alternative pair of first and second substrate bonding pads to form an electrically conductive path.--

--30. (New) The method according to claim 29, wherein the second set of alternative substrate electrical contacts corresponding to the second inductance circuit comprises alternative pairs of third and fourth substrate bonding pads positioned at variable locations on or within the package substrate, each of the third and fourth substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a sixth conductive feature, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth solder

bumps positioned so that they are electrically coupled to a selected respective alternative pair of third and fourth substrate bonding pads to form an electrically conductive path.--

--31. (New) The method according to claim 26, wherein the first set of alternative substrate electrical contacts corresponding to the first inductance circuit comprises alternative pairs of first and second substrate bonding pads positioned at variable locations on or within the package substrate, each of the first and second substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a fifth conductive feature, and wherein the first and second conductive features of the first inductance circuit comprise first and second wire bonds electrically coupled to a selected respective alternative pair of first and second substrate bonding pads to form an electrically conductive path.--

--32. (New) The method according to claim 31, wherein the second set of alternative substrate electrical contacts corresponding to the second inductance circuit comprises alternative pairs of third and fourth substrate bonding pads positioned at variable locations on or within the package substrate, each of the third and fourth substrate bonding pads of a bonding pad pair being electrically coupled to one another on or within the package substrate by a sixth conductive feature, and wherein the third and fourth conductive features of the second inductance circuit comprise third and fourth wire bonds

electrically coupled to a selected respective alternative pair of third and fourth substrate bonding pads to form an electrically conductive path.--

--33. (New) The method according to claim 26, further comprising providing a phase locked loop circuit within the integrated circuit, the phase locked loop circuit being electrically coupled to the first and second inductance circuits.--

--34. (New) The method according to claim 33, further comprising including a controlled oscillator circuit within the phase locked loop circuit.--

--35. (New) The method according to claim 34, wherein the controlled oscillator circuit has an output frequency that is selectably operable within a plurality of frequency bands.--

--36. (New) The method according to claim 35, wherein the controlled oscillator circuit comprises an inductor-capacitor tank circuit.--

--37. (New) The method according to claim 36, wherein the inductor-capacitor tank circuit comprises a capacitor electrically coupled to the first and second inductance circuits.--

--38. (New) The method according to claim 37, wherein the first and second inductance circuits are formed entirely within the semiconductor package.--

--39. (New) The method according to claim 26, wherein the first and second inductance circuits are formed symmetrically with respect to each other.--